Device reliability study of GaN HEMTs using low frequency noise measurements

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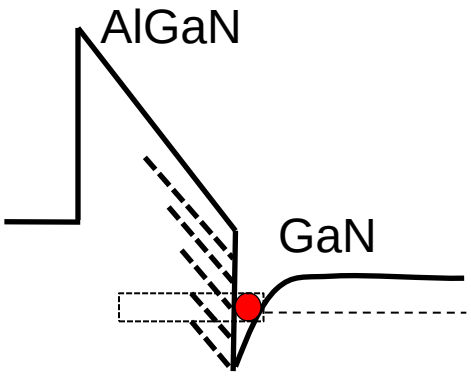
Motivation

- Excellent material properties of III-nitride heterostructures.
- Excellent demonstrated performance of AlGaN/GaN HEMTs.
  - High power ~ 13 W/mm
  - High frequency ~ 300 GHz
  - High breakdown voltage ~ 100 V
  - Integration with Si CMOS
- Multitude of short term performance degradation issues.
  - RF output power degradation
  - Current collapse
  - Threshold voltage shifts

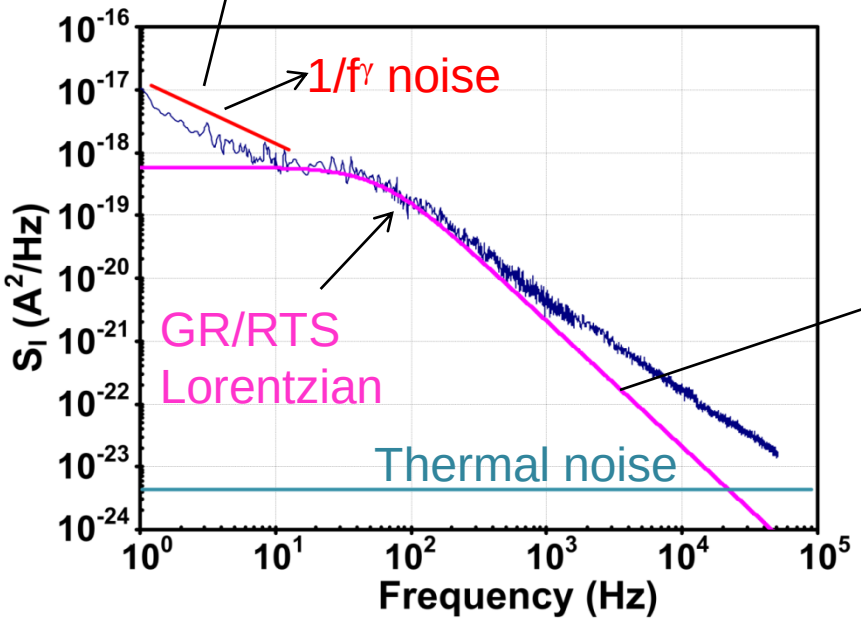
Outline

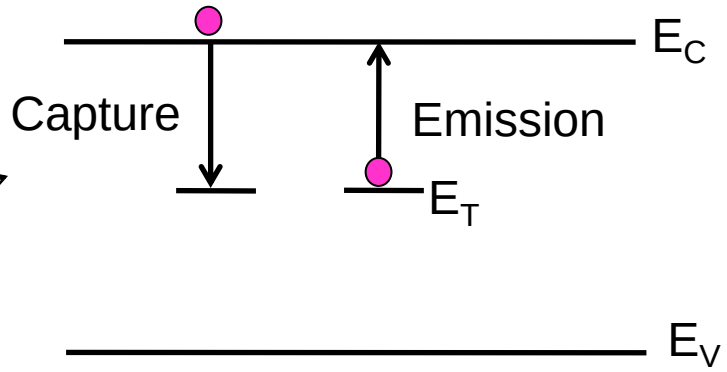
- Introduction
- Experimental details
- Short-term DC stress experiment
  - Gate electric field stress
  - Channel electrical field stress
- Results and analysis
- Conclusions

Defect spectroscopy via LFN noise



- Electrically benign and non-destructive trap characterization technique.
- Probes traps which directly affect the charge transport
- $1/f^{\gamma}$ noise gives *interface defect* quality information
- RTS and GR related Lorentzians give *point defect* information.

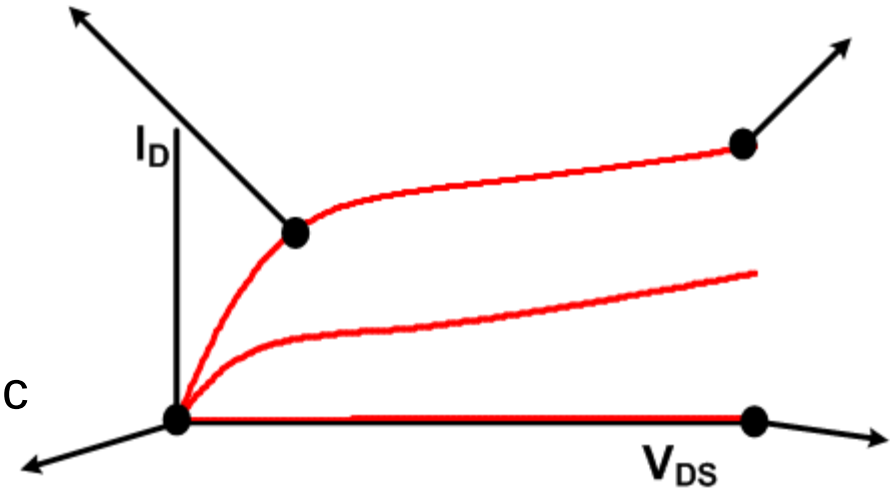




Stress effects in GaN HEMTs

Self-Heating
(Temperature effects)

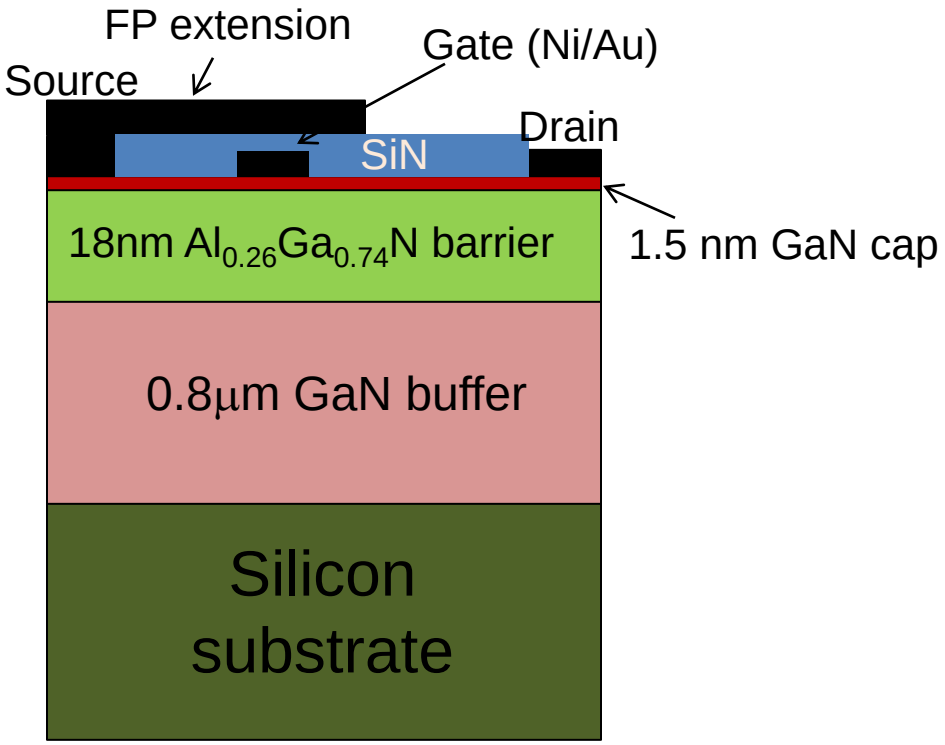
Self-Heating and
Hot-carriers



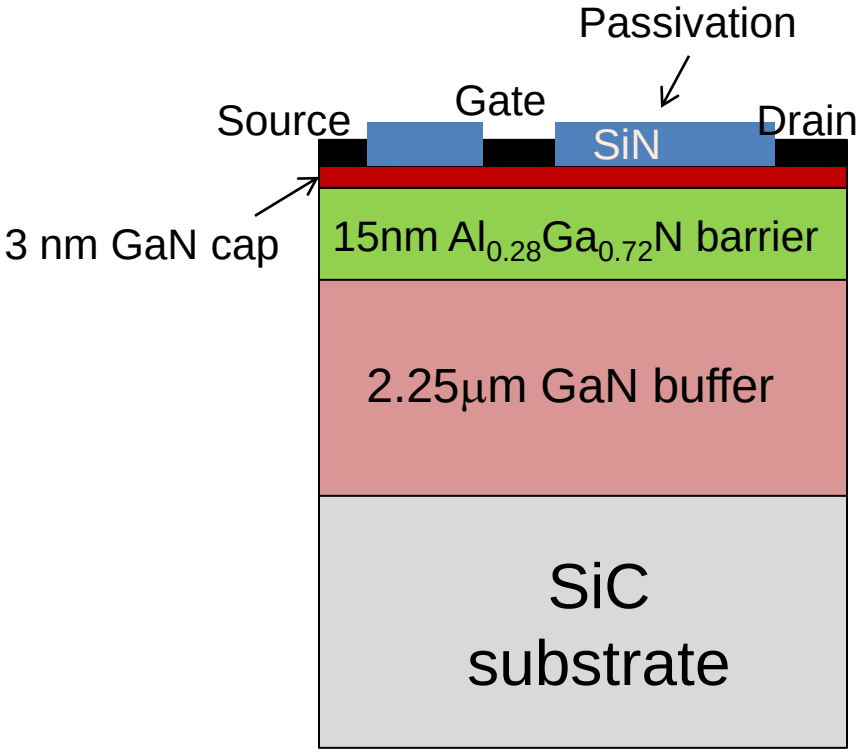
Inverse-Piezo electric stress (via large negative V_{GS} with V_{DS}=0 and I_D=0)

Hot-carriers

Devices under study

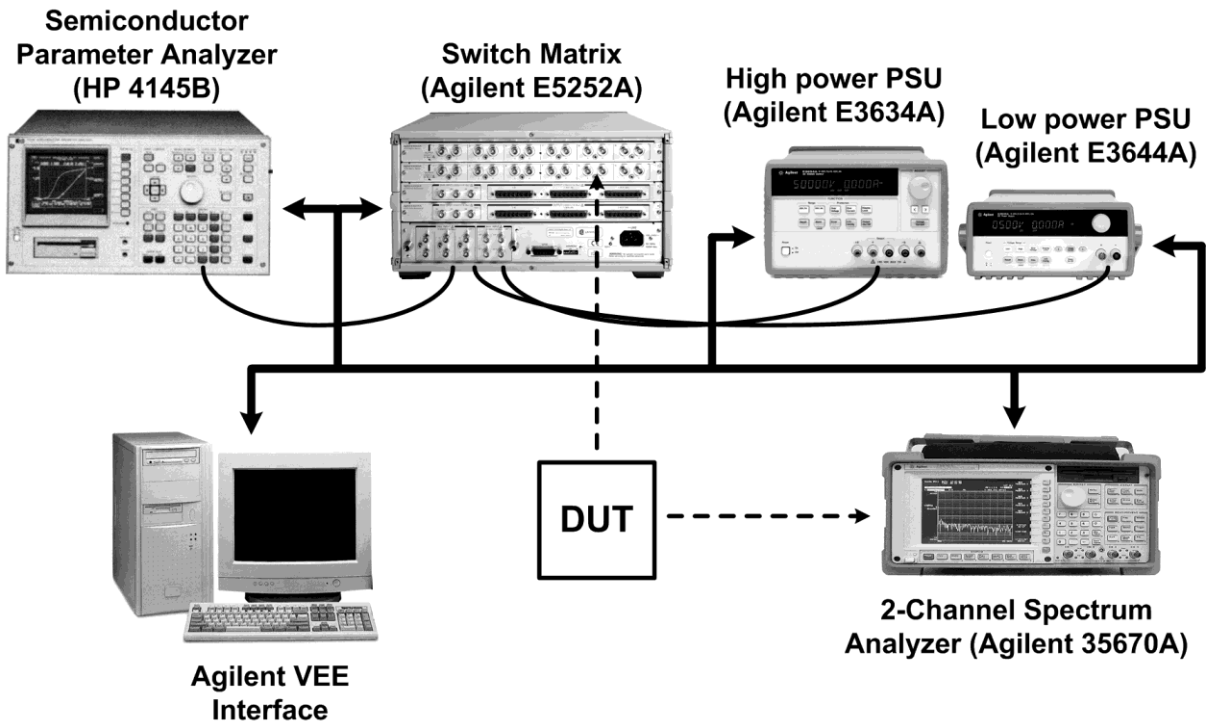


- Commercial device
- Gate length (L_G ~ 0.65 μm)
- 10 gate finger device with 2 mm periphery.
- Ceramic packaged.



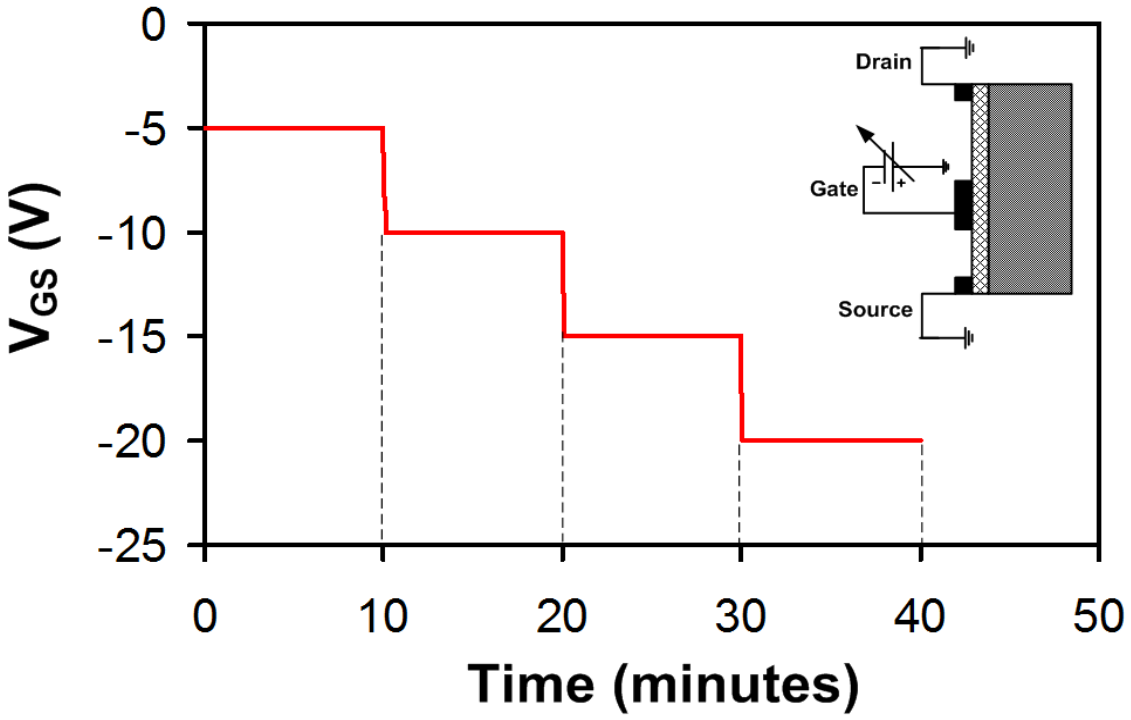
- AFRL sample
- Gate length (L_G ~ 0.1 μm)
- 2 gate finger device with W_G ~ 160 μm
- Ceramic packaged.

Stress measurement setup



- Simultaneous DC high current (~ 4A) and high voltage (~ 50V) stress capability.
- Trap spectroscopy capability via gate and channel LFN measurement.
- Fully automated for stress, DC and noise measurements.

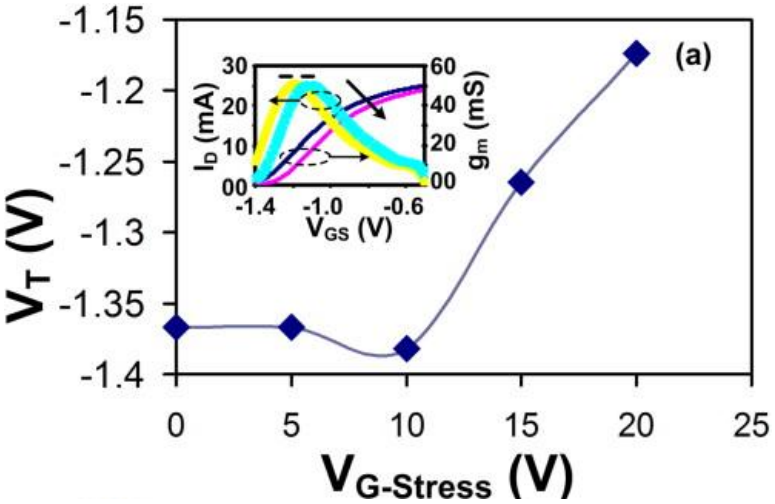
Gate stress experiment



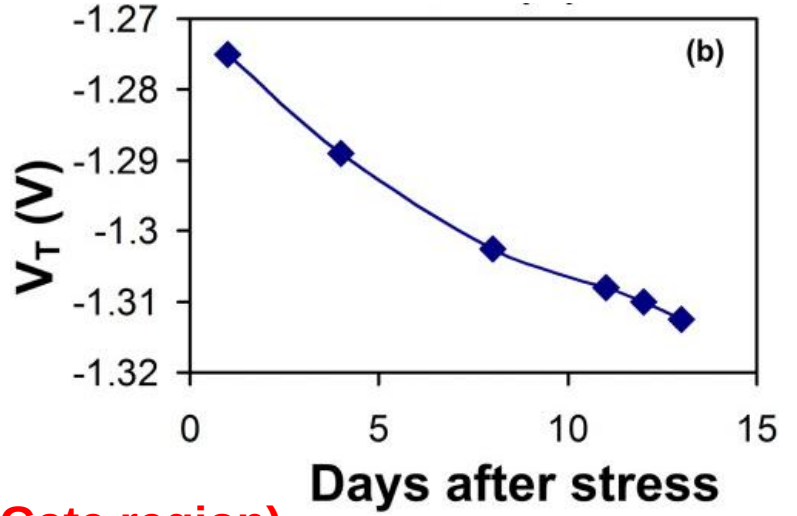
- Gate stack stressed from -5V to -20V for 10 minutes each with drain and source grounded.
- Transconductance I_G,I_D-V_G measured at the start of each stress bias. Drain and Gate current noise measured before and after stress.
- Device disconnected from the bias supplies after stress. Noise and I-V measurements continued for several weeks thereafter.

DC trap-related transient effects

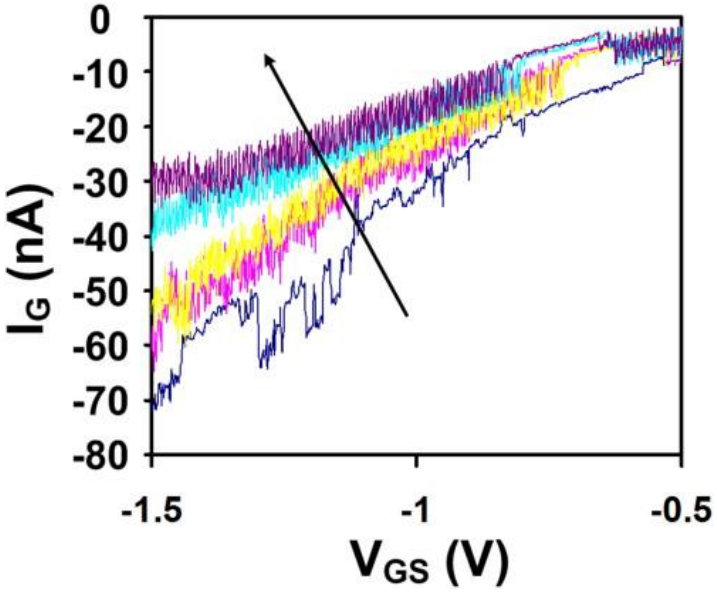
During stress (channel region)



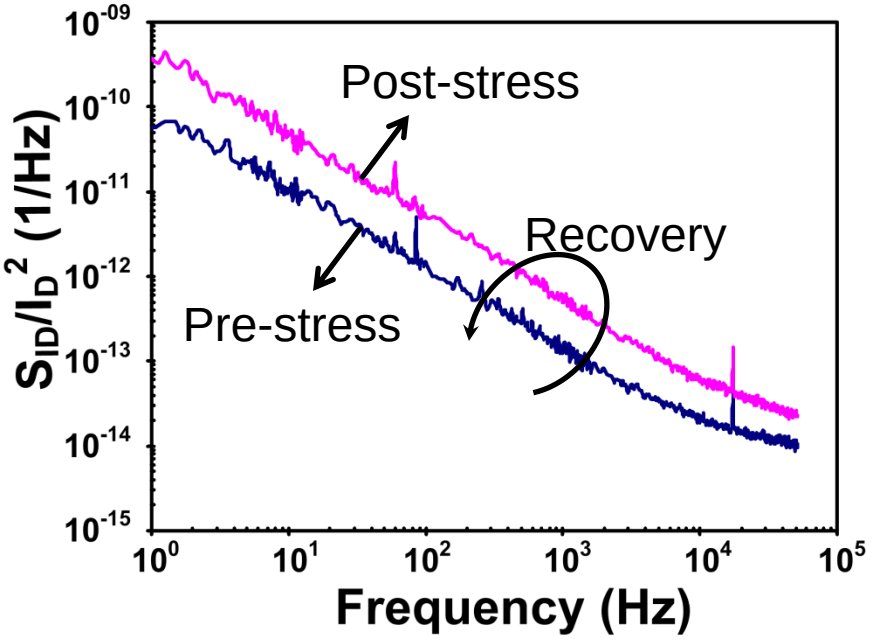
After stress (Channel region)



During stress (Gate region)



Channel noise evolution



$$\because \frac{S_{I_D}}{I_D^2} \cong \frac{S_{R_{CH}}}{R_{CH}^2} = \frac{\alpha_{CH}}{N_{CH} f}$$

$$Where, N_{CH} = C_{AlGaN}(V_{GS} - V_T)$$

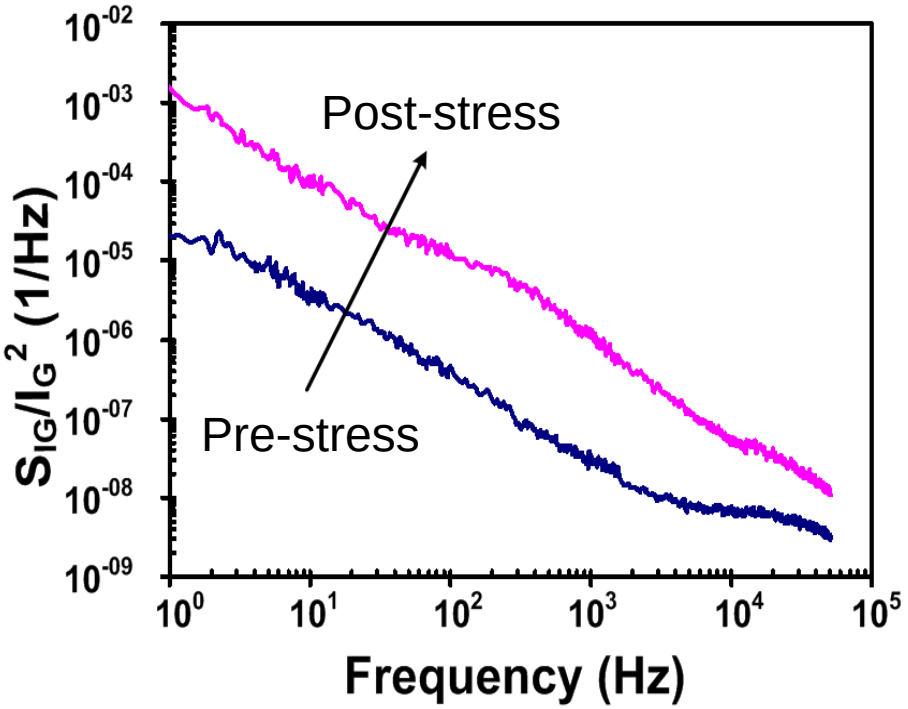
$\because V_{GS}$ is constant

$$\therefore V_T \downarrow \Rightarrow N_{CH} \uparrow \Rightarrow \frac{S_{I_D}}{I_D^2} \downarrow$$

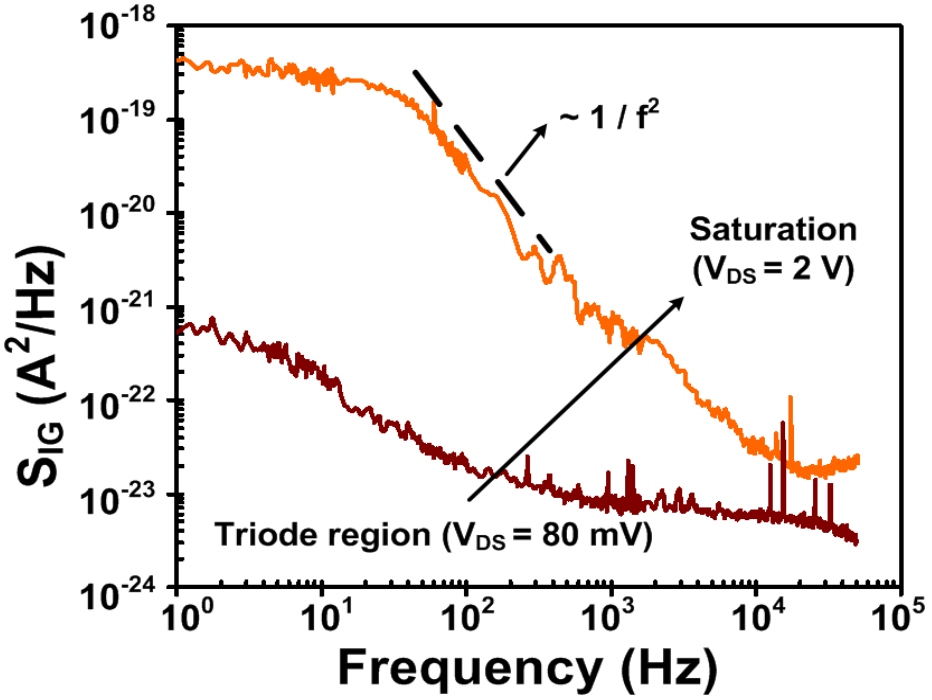
- No permanent channel degradation due to stress
- Threshold voltage shift causes temporary drain noise increase and recovery, during and after stress respectively

Gate noise evolution

Permanent Trap Creation

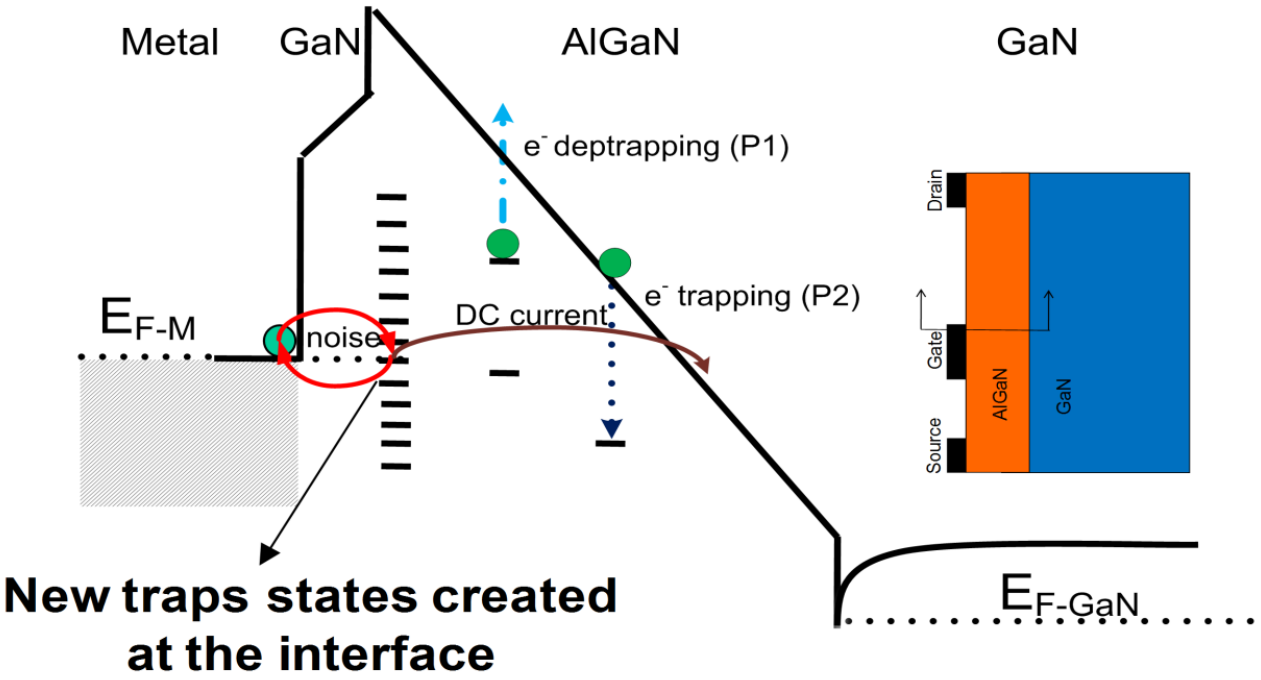


Trap location



- Permanent trap density increase of ~ 10x
- Increase of trap density is located at the gate edges

Degradation model



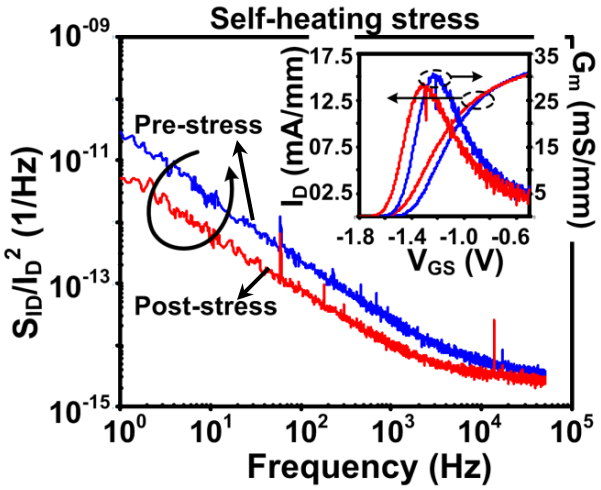
- New trap states are created at the GaN/AlGaN semiconductor interface during stress which leads to gate noise increase. Inverse piezo-electric effect is the possible explanation since very small gate current densities (~0.038 A/mm2) are involved during stress.
- Trap levels at the E_{F-M} quasi-Fermi level are likely candidates for modulating the trap assisted gate stack tunneling current.
- The DC transient effects are due to trap filling during stress and trap emptying after stress.

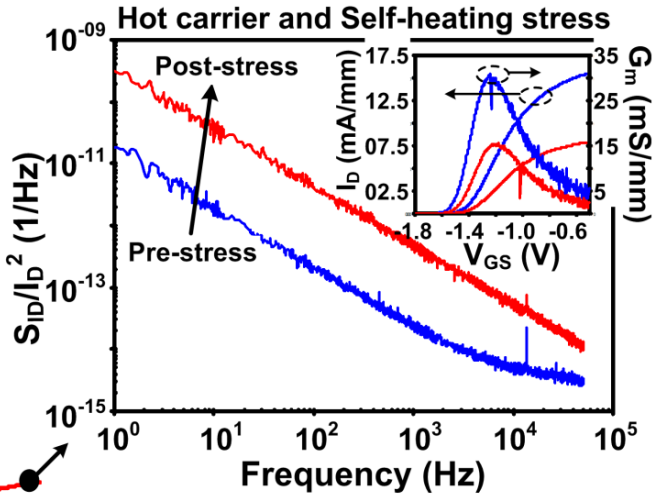
Channel stress experiment (GaN-on-Si)

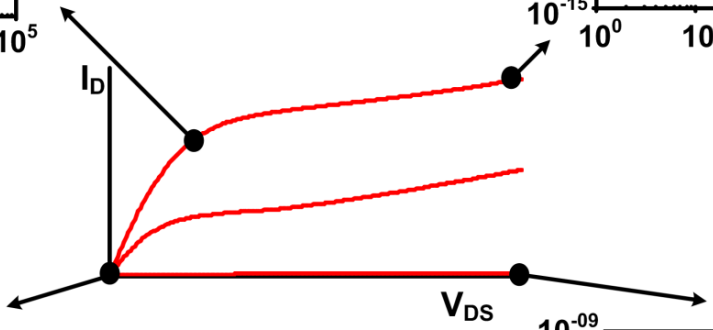
Test	V_{DS} (V)	V_{GS} (V)	P_{Dmax} (channel)	Stress time	Stress type
I	20	-1.7	2.3 W/mm	5 minutes	Hot carrier and self-heating
II	2	2	0.575 W/mm	30 minutes	Self-heating
III	10 to 30 step	-4	0.45 mW/mm	60 minutes	Hot-carrier

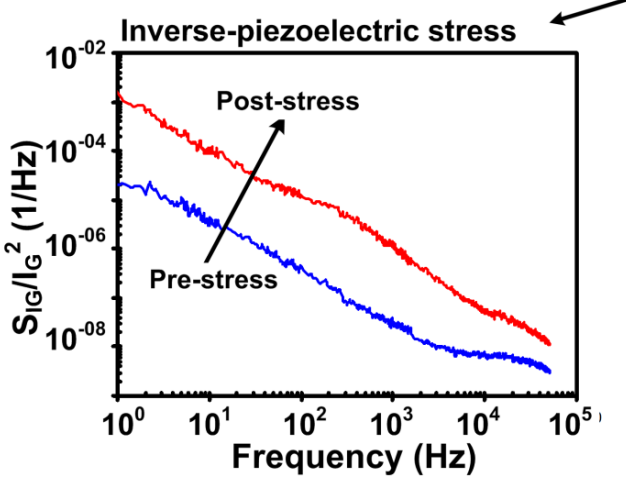
- Gate and Channel voltage are biased in the three critical DC bias points to invoke Hot-carrier, Self-heating and combined stress
- Transient and permanent changes in DC characteristics are monitored
- Trap spectroscopy is performed by gate and drain LFN measurement

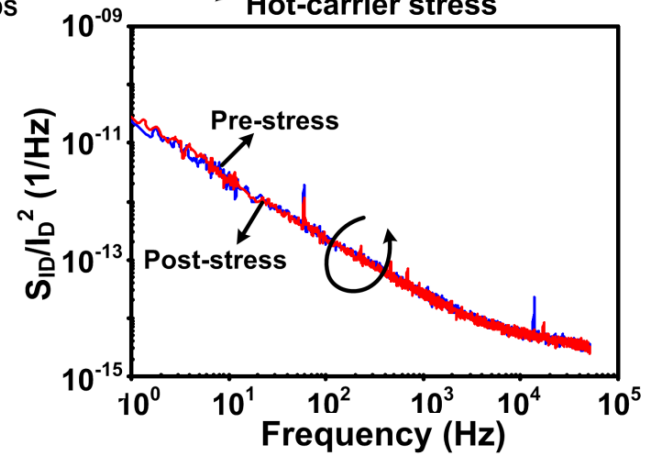
Results


Self-heating stress
Pre-stress
Post-stress
S_{ID}/I_D^2 (1/Hz)
Frequency (Hz)
I_D (mA/mm)
G_m (mS/mm)
V_{GS} (V)

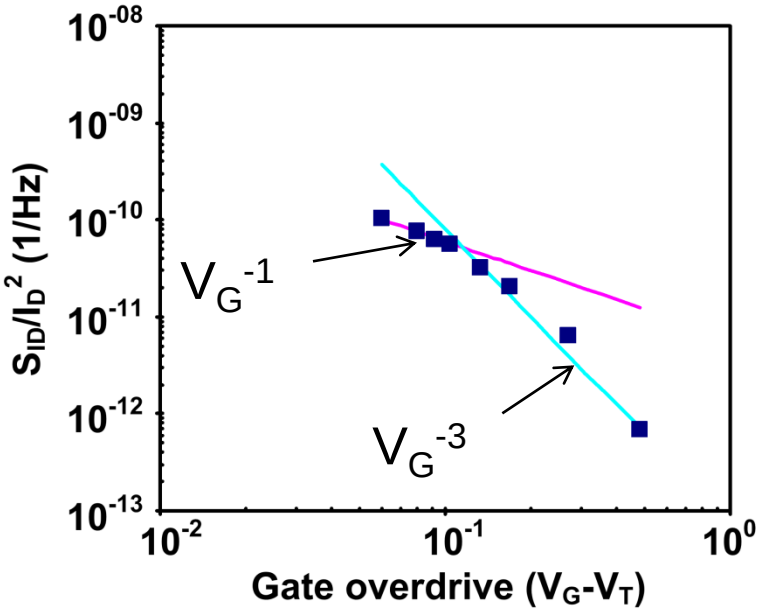

Hot carrier and Self-heating stress
Post-stress
Pre-stress
S_{ID}/I_D^2 (1/Hz)
Frequency (Hz)
I_D (mA/mm)
G_m (mS/mm)
V_{GS} (V)

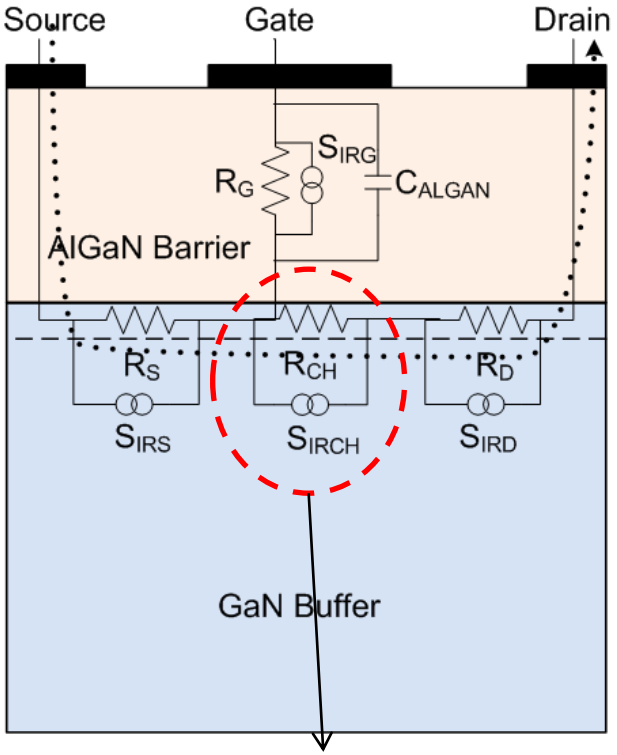

I_D
V_{DS}


Inverse-piezoelectric stress
Post-stress
Pre-stress
S_{IG}/I_G^2 (1/Hz)
Frequency (Hz)


Hot-carrier stress
Pre-stress
Post-stress
S_{ID}/I_D^2 (1/Hz)
Frequency (Hz)

Analysis

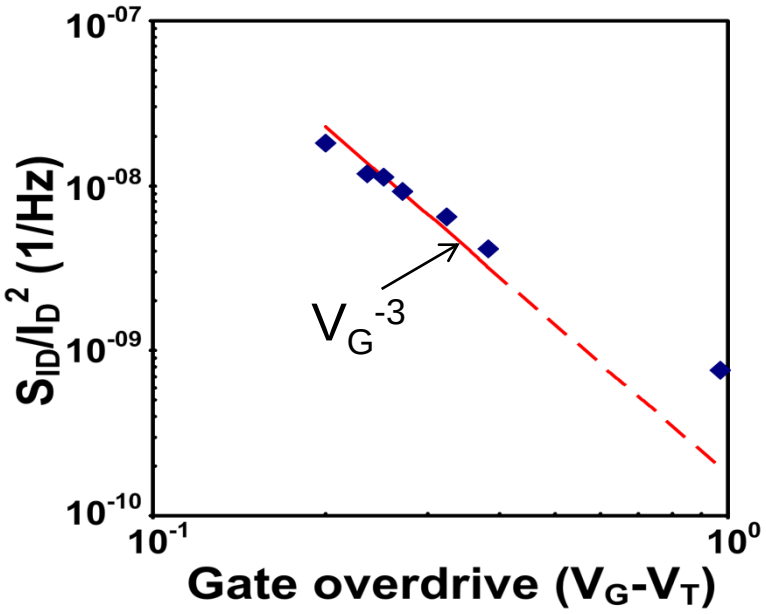


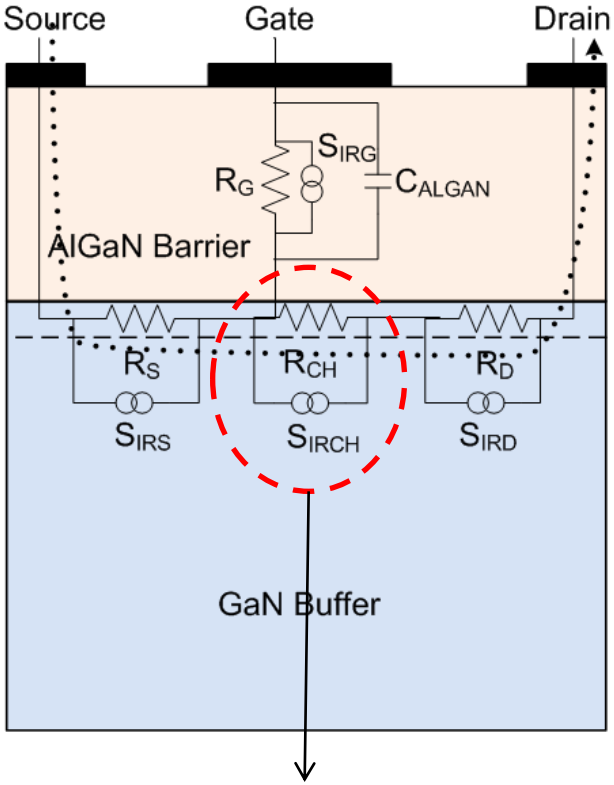


Degradation in the gated channel

- Increase of trap density at the AlGaN/GaN interface.
- ~ 15x degradation in the Hooge parameter (α_H) changing from ~ 10^{-3} to 1.5 × 10^{-2}

Channel stress experiment (GaN-on-SiC)





Degradation in the gated channel

- Hot carrier and self-heating stress at V_{DS} = 25V, V_{GS}=0, T=160s and P_D=18.75 W/mm
- ~ 84x degradation in the Hooge parameter (α_H) changing from 10^{-3} to 8.4 × 10^{-2}
- Localized increase of series access resistance due to transient trapping effect

Conclusions

- Characterized permanent trap creation and migration in the gate stack after high electric field stress.
- Characterized permanent degradation in the AlGaN/GaN interface after high electric field and self-heating stress.